Microtronix
ViClaro III HD Display Panel
Video IP Development Kit

USER MANUAL
REVISION 1.6

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Document Revision History

This user guide provides basic information about using the Microtronix ViClaro III HD Display Panel Video Development Kit. The following table shows the document revision history.

Date	Rev	Description
Dec. 2007	1.0	Initial Release
March 2007	1.1	Updated doc for Genesys GL9714 PCIe PHY.
March 2007	1.2	Added information on reference projects.
April 2008	1.3	Changes for rev D of ViClaro III Host Video board. Minor edits. Add PCIe benchmark section.
June 2008	1.4	Updated doc for HDMI Rx/Tx board.
July 2008	1.5	Pinout Updates
December 2008	1.6	Updated reference design information to reflect new designs in release 2.0

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Software updates to the ViClaro III Development Kit and supporting Microtronix IP Cores are listed on the download page of our website and made available via an email request form. Some product upgrades are only available to customers who have purchased the ViClaro III kit.

The upload site is for sending files to Technical Support.

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Typographic Conventions

Path/Filename	A path/filename
`[SOPC Builder]$ <cmd>`	A command that should be run from within the Cygwin Environment.
`Code`	Sample code.
↵	Indicates that there is no break between the current line and the next line.

Table of Contents

Introduction

The Microtronix ***ViClaro III HD Display Panel Video IP Development Kit*** is targeted at the development of consumer video display and imaging systems. It is designed to demonstrate the capabilities of Altera's Cyclone III for video and image enhancements applications in Video Display Controller ASSP systems.

The key features of the kit include:

- Altera Cyclone III FPGA (EP3C120F780C7N)
- 256 Mbyte DDR2 SDRAM (32 Meg x 64)
- 4-Lane PCI Express PHY
- USB 2.0 PHY
- I^2C interface port
- 3 High Speed Mezzanine Connectors (HSMC)
- Spread-spectrum crystal multiplier
- Quad Link LVDS Interface Card
- DVI Rx/Tx or HDMI Rx/TX Board.

Kit Contents

The Microtronix ***ViClaro III HD Display Panel Video IP Development Kit*** includes the following hardware components:

- ViClaro III Host Board (PN: 6252-00-00)
- Quad Link LVDS Interface Daughter Card (PN: 6253-01-01)
    - Mounting hardware
    - 2 – LVDS Loopback Cables (PN: 811-DF1340)
- DVI (PN: 6252-20-00) or HDMI (PN: 6256-20-00) Receiver / Transmitter Board
    - Mounting hardware
- USB Blaster
- 100-240 VAC - 12VDC Power Adapter (PN: 589-PS-1213AP)
- Microtronix ViClaro III Design Kit – Installation CD

Overview

A picture of the ***ViClaro III Host board*** with the ***Quad Link LVDS Interface card*** is shown in the following figure 1. The DVI Receiver / Transmitter Board is shown in the next figure 2.

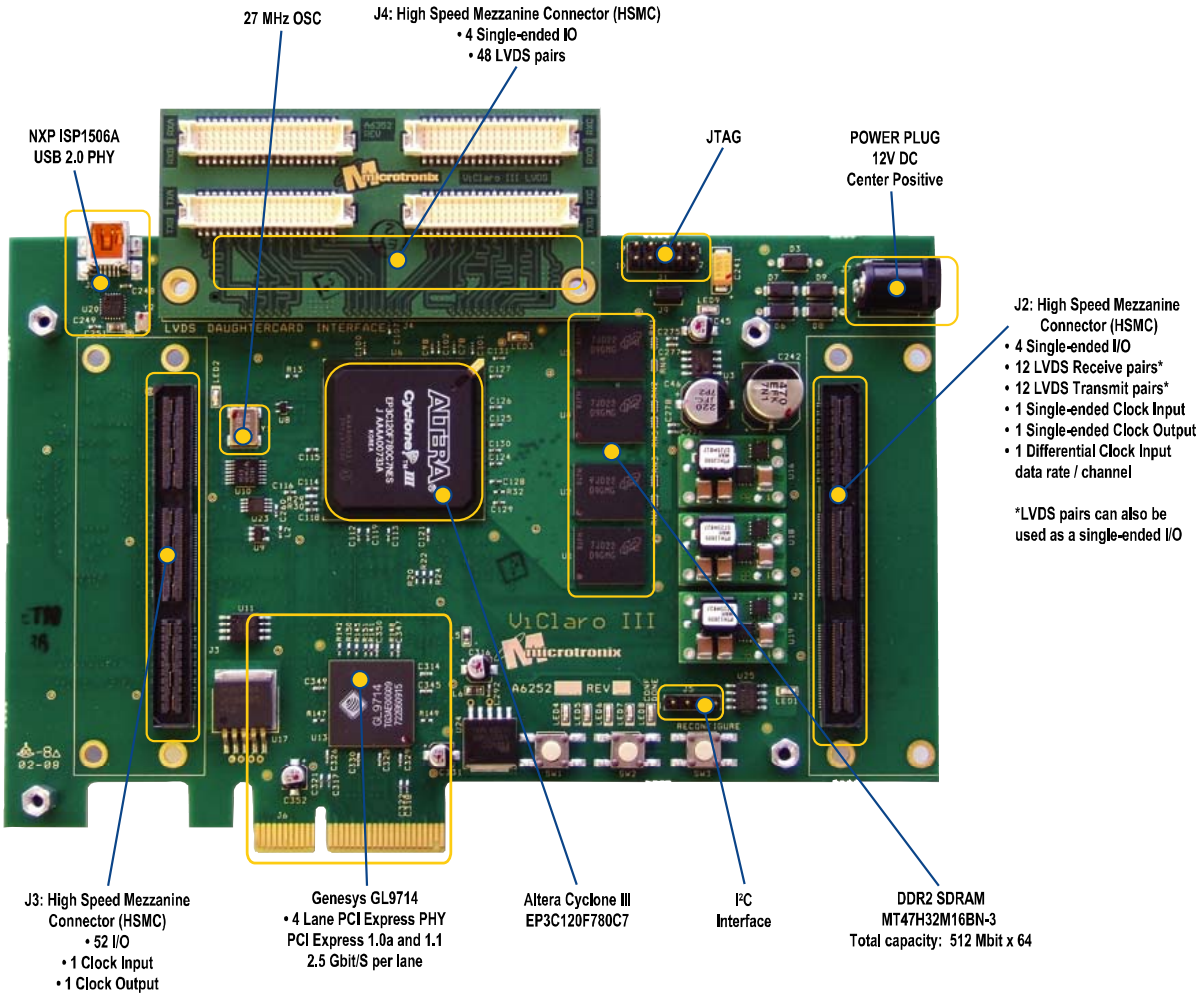

Figure 1: ViClaro Host Video Board with LVDS Daughter Card

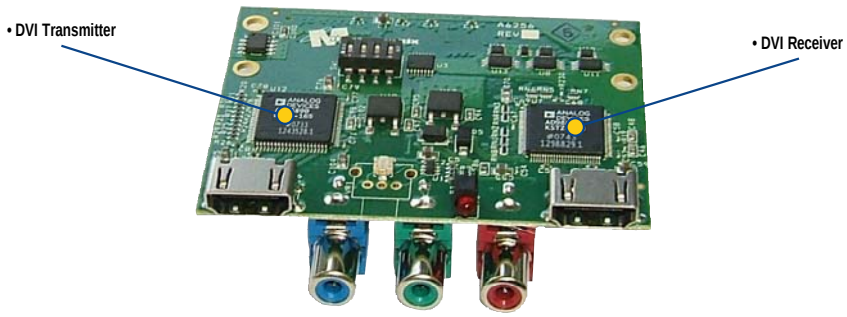

Figure 2: ViClaro HDMI Receiver / Transmitter Board

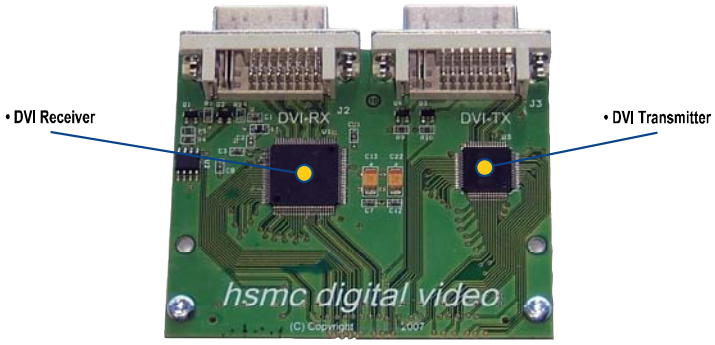

Figure 3: ViClaro DVI Receiver / Transmitter Board

Power Supply

The switching power modules generate 1.8V, 2.5V and 3.3V power levels. Linear regulators generate 1.2V and 5V required for the Cyclone III and I^2C.

The board is powered either from the 12V rail of a PCIe bus or from the 2.5mm power jack input using an external +12V DC power supply. The jack is polarity insensitive.

Power Consumption

The ViClaro board draws 1.5 A at 12 VDC. Power consumption varies according to the frequency of operation and amount of logic incorporated into the FPGA device.

Configuration

The Cyclone III device can be configured in JTAG stand-alone mode or passive serial mode. At power-up the MAXII PLD configures the Cyclone III device from the on-board flash. If the configuration is successful, the CONF_DONE LED illuminates. Pressing SW3 will reload the FPGA with the design stored in flash.

For instructions on programming the FPGA via JTAG, see Appendix A. The flash can be programmed using JTAG in-system programming. See Appendix B.

Clocking

The board has a 27 MHz crystal oscillator. Figure 2 shows the clocking circuitry.

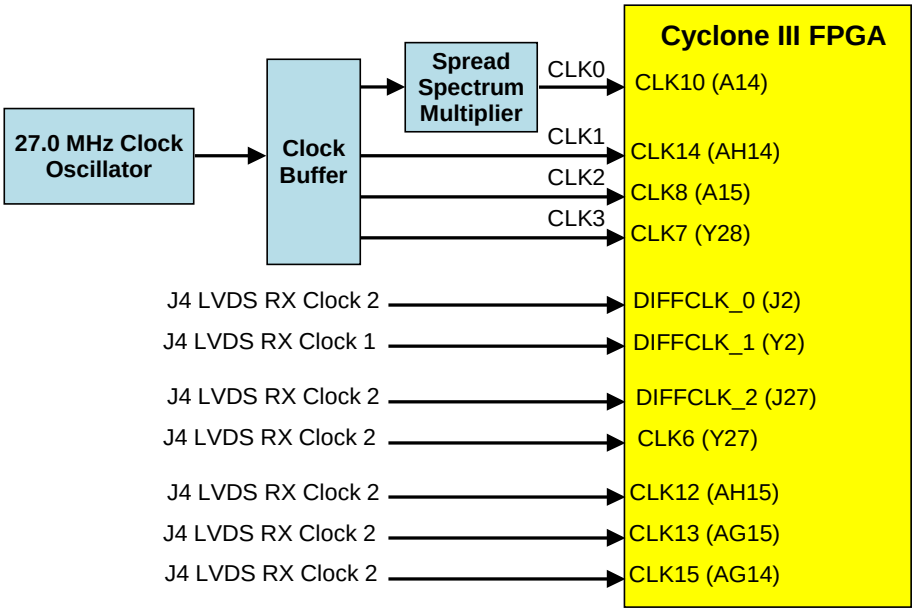

Figure 3: Clock Circuitry

Spread-Spectrum Clock Multiplier

A DS1080L, Spread-Spectrum Clock (SS) Multiplier (U23) is provided to facilitate spread-spectrum clocking of LVDS transmit data. The SS magnitude is set to ±1.5% with a clock multiplier of 1X.

ViClaro III Host Board Components

Cyclone III

The ViClaro III Host board is fitted with an Altera Cyclone III EP3C120 device in a 780-pin Fine Line BGA package with speed grade -7. See appendices A and B for instructions on programming the FPGA.

For more information on Cyclone III devices, refer to the Altera Cyclone III Device Handbook.

User LEDs

There are four general purpose LEDs driven by the Cyclone III device. The LEDs are located in bank 7. The I/O standard for these pins should be set to 1.8V.

Table 1: Cyclone III – LED pin assignments

LED	Pin Number
LED7	E25
LED6	E24
LED5	G22
LED4	D24

User Buttons

There are two general-purpose buttons driving inputs on the Cyclone III device. The buttons are located in bank 7. The I/O standard for these pins should be set to 1.8V.

Table 2: Cyclone III – Switch /push button pin assignments

Switch	Pin Number
SW1	G21
SW2	H21

I^2C Interface Header

The ViClaro III Host board has an I^2C interface (J5), which can be used to access the (optional) I^2C controller / slave in the Cyclone III. It also provides access to the HSMC I^2C interfaces. The interface has two level shifters, so an external I^2C master can be connected without damaging the Cyclone III device. In addition a 5-volt power supply and pull-up resistors are provided. The I/O standard for these pins should be set to 2.5V.

Table 3: Cyclone III – I2C Pin assignments

Description	Pin Number
SCL	AA10
SDA	Y10

DDR2 SDRAM

The ViClaro III board has four Micron DDR2 SDRAM devices (MT47H16M16BG-3) with a total capacity of 32M x 64. The memory devices are connected to banks 7 and 8 of the Cyclone III device and use the SSTL-18 I/O-standard. The two banks are powered with the

1.8V power supply. The board is designed for matched length traces across all DDR2 signals. All unused I/O-pins in the banks are connected to ground.

There are two clock outputs from the FPGA to the four devices. The lower 32 bits (U5, U4) use CLK0/CLK#0 and the upper 32 bits (U2, U1) use CLK1/CLK#1.

The DDR2 SDRAM has been tested at 167 MHz (333 MT/s) using the Microtronix Streaming and Avalon SDRAM Memory Controller IP cores.

Table 4: Cyclone III – DDR2 SDRAM key pin assignments

Signal Name	Pin Number	Signal Name	Pin Number
CKE	G11	A0	J12
CS#	G16	A1	H12
RAS#	F11	A2	J13
CAS#	G18	A3	H13
WE#	G13	A4	J14
ODT	G20	A5	H14
		A6	J15
		A7	H15
		A8	J16
		A9	H16
		A10	J17
BA0	H19	A11	H17
BA1	G19	A12	J19

Table 5: Cyclone III – DDR2 SDRAM key pin assignments

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
DQ0	A3	DQ17	A11	DQ32	E17	DQ48	E18
DQ1	A4	DQ17	A12	DQ33	C16	DQ49	D21
DQ2	C4	DQ18	B11	DQ34	C17	DQ50	C21
DQ3	D6	DQ19	C12	DQ35	B18	DQ51	B21
DQ4	C6	DQ20	C13	DQ36	A19	DQ52	A21
DQ5	C7	DQ21	C14	DQ37	B19	DQ53	A22
DQ6	C8	DQ22	D13	DQ38	C19	DQ54	C22
DQ7	D8	DQ23	E14	DQ39	D20	DQ55	C24
DQ8	A7	DQ24	E8	DQ40	F15	DQ56	F21
DQ9	B6	DQ25	F8	DQ41	C15	DQ57	E22
DQ10	B7	DQ26	G8	DQ42	D15	DQ58	D22
DQ11	C9	DQ27	H8	DQ43	A17	DQ59	A23
DQ12	C10	DQ28	F10	DQ44	A18	DQ60	C25
DQ13	C11	DQ29	G10	DQ45	D16	DQ61	B25
DQ14	D10	DQ30	H10	DQ46	D18	DQ62	B26
DQ15	E11	DQ31	J10	DQ47	D19	DQ63	A26
DQS0	B4	DSQ2	D12	DQS4	B17	DQS6	D17
DQS1	E12	DQS3	F7	DQS5	F18	DQS7	A25
DM0	D4	DM2	B10	DM4	E15	DM6	C20
DM1	A8	DM3	E7	DM5	F17	DM7	B23
CLK0	D5			CLK1	D23		
CLK#	C5			CLK#1	C23		

Notes:

1) The Microtronix SDRAM Memory Controller IP cores use source synchronous DQS clocking to capture data from the DDR2 memory devices and does not require the use of dedicated DQ pins for the data. The IO banks used for DDR2 memory only provided 48 bits of DQ pins, however, the Microtronix core can support a full 64-bit memory interface by using non-dedicated IO for the DQ signals.
2) The Altera memory controller requires DQ signals to be on DQ pins and is therefore limited to a 32-bit memory interface on the ViClaro III board. To accommodate this core, the low 8-bits of each chip are all connected to the dedicated DQ pins and used to provide a 32-bit interface.

PCI Express PHY

The ViClaro III board contains a Genesys GL9714 PCI Express stand-alone 4-lane (x4) PHY (U13). The PCI Express interface pins are located in banks 4 and 5. These banks are powered at 2.5 volts and use the SSTL-2 I/O standard. For more information see the Genesys GL9714 datasheet.

Table 6: PCI Express PHY Common Pins

Signal Name	Pin Number	Signal Name	Pin Number
PCI_RX_CLK	AG15	PCI_PWRDWN0	AB25
PCI_TX_CLK	*	PCI_PWRDWN1	AC25
PCI_PHYSTATUS	AG21	PCI_RESET_N	AC24
PCI_RXDET_LOOPB	AA24	PCI_SMC*	AE23
		PCI_SMD	AB16

* The forthcoming GL9714S version uses the same pin for PCI_SMC & PCI_TX_Clk.

Table 7: PCI Express PHY Lane 0 Pins

Signal Name	Pin Number	Signal Name	Pin Number
PCI_L0_RXDATA0	AB22	PCI_L0_TXDATA0	V28
PCI_L0_RXDATA1	AA21	PCI_L0_TXDATA1	U28
PCI_L0_RXDATA2	AC22	PCI_L0_TXDATA2	R28
PCI_L0_RXDATA3	AC21	PCI_L0_TXDATA3	R27
PCI_L0_RXDATA4	AB21	PCI_L0_TXDATA4	U27
PCI_L0_RXDATA5	Y19	PCI_L0_TXDATA5	R26
PCI_L0_RXDATA6	AB19	PCI_L0_TXDATA6	U26
PCI_L0_RXDATA7	AA19	PCI_L0_TXDATA7	T26
PCI_L0_RXDATAK	AD18	PCI_L0_TXDATAK	V27
PCI_L0_RXPOL	AD25	PCI_L0_TXIDLE	W27
PCI_L0_RXVALID	AD24	PCI_L0_TXCOMP	W28
PCI_L0_RXIDLE	AC19		
PCI_L0_RXSTATUS0	AD22		
PCI_L0_RXSTATUS1	AD21		
PCI_L0_RXSTATUS2	AD19		

Table 8: PCI Express PHY Lane 1 Pins

Signal Name	Pin Number	Signal Name	Pin Number
PCI_L1_RXDATA0	AG22	PCI_L1_TXDATA0	AB27
PCI_L1_RXDATA1	AF22	PCI_L1_TXDATA1	AD26
PCI_L1_RXDATA2	AH22	PCI_L1_TXDATA2	AE26
PCI_L1_RXDATA3	AF24	PCI_L1_TXDATA3	AD27
PCI_L1_RXDATA4	AH23	PCI_L1_TXDATA4	AE27
PCI_L1_RXDATA5	AH25	PCI_L1_TXDATA5	AF27
PCI_L1_RXDATA6	AG25	PCI_L1_TXDATA6	AD28
PCI_L1_RXDATA7	AH26	PCI_L1_TXDATA7	AE28
PCI_L1_RXDATAK	AG26	PCI_L1_TXDATAK	AB28
PCI_L1_RXPOL	AE22	PCI_L1_TXIDLE	AC27
PCI_L1_RXVALID	AG23	PCI_L1_TXCOMP	AC28
PCI_L1_RXIDLE	AF26		
PCI_L1_RXSTATUS0	AE24		
PCI_L1_RXSTATUS1	AF25		
PCI_L1_RXSTATUS2	AE25		

Table 9: PCI Express PHY Lane 2 Pins

Signal Name	Pin Number	Signal Name	Pin Number
PCI_L2_RXDATA0	AE18	PCI_L2_TXDATA0	V23
PCI_L2_RXDATA1	AE19	PCI_L2_TXDATA1	V24
PCI_L2_RXDATA2	AF18	PCI_L2_TXDATA2	W25
PCI_L2_RXDATA3	AF17	PCI_L2_TXDATA3	Y26
PCI_L2_RXDATA4	AG17	PCI_L2_TXDATA4	Y25
PCI_L2_RXDATA5	AH17	PCI_L2_TXDATA5	Y24
PCI_L2_RXDATA6	AG18	PCI_L2_TXDATA6	Y23
PCI_L2_RXDATA7	AH18	PCI_L2_TXDATA7	AA23
PCI_L2_RXDATAK	AH19	PCI_L2_TXDATAK	W26
PCI_L2_RXPOL	AE21	PCI_L2_TXIDLE	V25
PCI_L2_RXVALID	AF20	PCI_L2_TXCOMP	V26
PCI_L2_RXIDLE	AG19		

PCI_L2_RXSTATUS0	AF21		
PCI_L2_RXSTATUS1	AE20		
PCI_L2_RXSTATUS2	AF19		

Table 10: PCI Express PHY Lane 3 Pins

Signal Name	Pin Number	Signal Name	Pin Number
PCI_L3_RXDATA0	Y16	PCI_L3_TXDATA0	R24
PCI_L3_RXDATA1	AA16	PCI_L3_TXDATA1	R25
PCI_L3_RXDATA2	AC17	PCI_L3_TXDATA2	R23
PCI_L3_RXDATA3	AA17	PCI_L3_TXDATA3	U22
PCI_L3_RXDATA4	AD17	PCI_L3_TXDATA4	U23
PCI_L3_RXDATA5	Y17	PCI_L3_TXDATA5	R22
PCI_L3_RXDATA6	AE15	PCI_L3_TXDATA6	T22
PCI_L3_RXDATA7	AF115	PCI_L3_TXDATA7	R21
PCI_L3_RXDATAK	AF16	PCI_L3_TXDATAK	T25
PCI_L3_RXPOL	AB18	PCI_L3_TXIDLE	U24
PCI_L3_RXVALID	AE17	PCI_L3_TXCOMP	U25
PCI_L3_RXIDLE	AE16		
PCI_L3_RXSTATUS0	AD15		
PCI_L3_RXSTATUS1	AC15		
PCI_L3_RXSTATUS2	AB17		

There is an additional signal from the PCI Express edge connector directly to the Cyclone III. Signal PCI_RST# is connected to pin AB15.

Table 11: PCI Express Card Edge Connector Pin Assignments

Pin	Signal Name		Pin	Signal Name	
	Side A	Side B		Side A	Side B
1	PRSNT1#	+12V	17	PERn0	PRSNT2#
2	+12V	+12V	18	GND	GND
3	+12V	+12V	19	RSVD	PETp1
4	GND	GND	20	GND	PETn1
5	JTAG2	SMCLK	21	PERp1	GND
6	JTAG3	SMDAT	22	PERn1	GND
7	JTAG4	GND	23	GND	PETp2
8	JTAG5	+3.3V	24	GND	PETn2
9	+3.3V	JTAG1	25	PERp2	GND
10	+3.3V	3.3Vaux	26	PERn2	GND
11	PERST#	WAKE#	27	GND	PETp3
12	GND	RSVD	28	GND	PETn3
13	REFCLK+	GND	29	PERp3	GND
14	REFCLK-	PETp0	30	PERn3	RSVD
15	GND	PETn0	31	GND	PRSNT2#
16	PERp0	GND	32	RSVD	GND

Connector J2, HSMC1

The ViClaro III board has three High Speed Mezzanine Connectors (HSMC). HSMC1 (J2) connector is located beside the power jack. It can be used for either single-ended signaling or differential.

In its default configuration, HSMC1 provides 52 I/Os. In addition, HSMC1 contains one dedicated clock input connected to PLL2.

With the optional differential termination resistors (R34-R46, 100ohm) installed, this connector provides 12 differential receive pairs and 12 differential transmit pairs. It also provides a differential clock input connected to PLL2.

The HSMC1 interface pins are located in bank 6 and this bank is powered at 2.5 volts. HSMC1_CLKIN0 is located in bank 5 and is also powered at 2.5 volts.

Table 12: J2, HSMC1 pin assignments

Cyclone III Pin #	Signal Name	HSMC Pin #	HSMC Pin #	Signal Name	Cyclone III Pin #
	NC	1	2	NC	
	NC	3	4	NC	
	NC	5	6	NC	
	NC	7	8	NC	
	NC	9	10	NC	
	NC	11	12	NC	
	NC	13	14	NC	
	NC	15	16	NC	
	NC	17	18	NC	
	NC	19	20	NC	
	NC	21	22	NC	
	NC	23	24	NC	
	NC	25	26	NC	
	NC	27	28	NC	
	NC	29	30	NC	
	NC	31	32	NC	
Y10	I2C_SDA	33	34	I2C_SLC	AA10
	NCJTAG_TCK	35	36	JTAG_TMS	
	NCJTAG_TDO	37	38	JTAG_TDI	
M24	HSMC1_CLKOUT0	39	40	HSMC1_CLKIN0	Y27

H22	HSMC1_D0	41	42	HSMC1_D1	J22
L25	HSMC1_D2	43	44	HSMC1_D3	L26
	3.3V	45	46	12V	
D26	HSMC_TX_p0	47	48	HSMC_RX_p0	D27
C27	HSMC_TX_n0	49	50	HSMC_RX_n0	D28
	3.3V	51	52	12V	
F26	HSMC_TX_p1	53	54	HSMC_RX_p1	E27
E26	HSMC_TX_n1	55	56	HSMC_RX_n1	E28
	3.3V	57	58	12V	
F24	HSMC_TX_p2	59	60	HSMC_RX_p2	F27
F25	HSMC_TX_n2	61	62	HSMC_RX_n2	F28
	3.3V	63	64	12V	
G25	HSMC_TX_p3	65	66	HSMC_RX_p3	G27
G26	HSMC_TX_n3	67	68	HSMC_RX_n3	G28
	3.3V	69	70	12V	
H23	HSMC_TX_p4	71	72	HSMC_RX_p4	G23
H24	HSMC_TX_n4	73	74	HSMC_RX_n4	G24
	3.3V	75	76	12V	
J25	HSMC_TX_p5	77	78	HSMC_RX_p5	H25
J26	HSMC_TX_n5	79	80	HSMC_RX_n5	H26
	3.3V	81	82	12V	
K21	HSMC_TX_p6	83	84	HSMC_RX_p6	J23
K22	HSMC_TX_n6	85	86	HSMC_RX_n6	J24
	3.3V	87	88	12V	
K25	HSMC_TX_p7	89	90	HSMC_RX_p7	K27
K26	HSMC_TX_n7	91	92	HSMC_RX_n7	K28
	3.3V	93	94	12V	
P25	CLKOUT1P	95	96	HSMC1_CLKIN1_P	J27
P26	CLKOUT1N	97	98	HSMC1_CLKIN1_N	J28
	3.3V	99	100	12v	
L21	HSMC_TX_p8	101	102	HSMC_RX_p8	L23
L22	HSMC_TX_n8	103	104	HSMC_RX_n8	L24
	3.3V	105	106	12V	
M27	HSMC_TX_p9	107	108	HSMC_RX_p9	L27
M28	HSMC_TX_n9	109	110	HSMC_RX_n9	L28

	3.3V	111	112	12V	
N25	HSMC_TX_p10	113	114	HSMC_RX_p10	M25
N26	HSMC_TX_n10	115	116	HSMC_RX_n10	M26
	3.3V	117	118	12V	
	NC	119	120	HSMC_RX_p11	P27
	NC	121	122	HSMC_RX_n11	P28
	3.3V	123	124	12V	
	NC	125	126	NC	
	NC	127	128	NC	
	3.3V	129	130	12V	
	NC	131	132	NC	
	NC	133	134	NC	
	3.3V	135	136	12V	
	NC	137	138	NC	
	NC	139	140	NC	
	3.3V	141	142	12V	
	NC	143	144	NC	
	NC	145	146	NC	
	3.3V	147	148	12V	
	NC	149	150	NC	
	NC	151	152	NC	
	3.3V	153	154	12V	
	NC	155	156	NC	
	NC	157	158	NC	
	3.3V	159	160	Presence LED*	

* Note: Connect to GND to turn LED on.

Connector J3, HSMC2

HSMC2 (J3) is located on the PCI chassis plate side of the board and provides 52 I/Os. In addition, HSMC2 contains one dedicated clock input and one dedicated output connected to PLL4.

The HSMC2 pins are located in bank 3 of the FPGA. This bank is powered at 2.5V.

Table 13: J3, HSMC2 pin assignments

Cyclone III Pin #	Signal Name	HSMC Pin #	HSMC Pin #	Signal Name	Cyclone III Pin #
	NC	1	2	NC	
	NC	3	4	NC	
	NC	5	6	NC	
	NC	7	8	NC	
	NC	9	10	NC	
	NC	11	12	NC	
	NC	13	14	NC	
	NC	15	16	NC	
	NC	17	18	NC	
	NC	19	20	NC	
	NC	21	22	NC	
	NC	23	24	NC	
	NC	25	26	NC	
	NC	27	28	NC	
	NC	29	30	NC	
	NC	31	32	NC	
Y10	I2C_SDA	33	34	I2C_SLC	AA10
	NC	35	36	NC	
	NC	37	38	NC	
AE5	HSMC2_CLKOUT0	39	40	HSMC_CLKIN0	AG14
AC14	HSMC2_D0	41	42	HSMC2_D1	AD14
AE14	HSMC2_D2	43	44	HSMC2_D3	ADF4
	3.3V	45	46	12V	
AB13	HSMC2_D4	47	48	HSMC2_D5	AE13
AF13	HSMC2_D6	49	50	HSMC2_D7	AA12
	3.3V	51	52	12V	
AB12	HSMC2_D8	53	54	HSMC2_D9	AC12
AD12	HSMC2_D10	55	56	HSMC2_D11	AE12
	3.3V	57	58	12V	
AF12	HSMC2_D12	59	60	HSMC2_D13	AG12
AH12	HSMC2_D14	61	62	HSMC2_D15	AB11
	3.3V	63	64	12V	

AC11	HSMC2_D16	65	66	HSMC2_D17	AD11
AE11	HSMC2_D18	67	68	HSMC2_D19	AF11
	3.3V	69	70	12V	
AG11	HSMC2_D20	71	72	HSMC2_D21	AH11
AB10	HSMC2_D22	73	74	HSMC2_D23	AC10
	3.3V	75	76	12V	
AD10	HSMC2_D24	77	78	HSMC2_D25	AE10
AF10	HSMC2_D26	79	80	HSMC2_D27	AG10
	3.3V	81	82	12V	
AH10	HSMC2_D28	83	84	HSMC2_D29	AB9
AE9	HSMC2_D30	85	86	HSMC2_D31	AF9
	3.3V	87	88	12V	
AA8	HSMC2_D32	89	90	HSMC2_D33	AB8
AC8	HSMC2_D34	91	92	HSMC2_D35	AD8
	3.3V	93	94	12V	
AE8	HSMC2_D36	95	96	HSMC2_D37	AF8
AG8	HSMC2_D38	97	98	HSMC2_D39	AH8
	3.3V	99	100	12v	
AB7	HSMC2_D40	101	102	HSMC2_D41	AC7
AD7	HSMC2_D42	103	104	HSMC2_D43	AE7
	3.3V	105	106	12V	
AF7	HSMC2_D44	107	108	HSMC2_D45	AG7
AH7	HSMC2_D46	109	110	HSMC2_D47	AE6
	3.3V	111	112	12V	
AF6	HSMC2_D48	113	114	HSMC2_D49	AG6
AH6	HSMC2_D50	115	116	HSMC2_D51	AD5
	3.3V	117	118	12V	
AF5	HSMC2_D52‡	119	120	HSMC2_D53‡	Y15
Y14	HSMC2_D54‡	121	122	HSMC2_D55‡	Y13
	3.3V	123	124	12V	
Y13	HSMC2_D56‡	125	126	HSMC2_D57‡	AA13
AB14	HSMC2_D58‡	127	128	NC	
	3.3V	129	130	12V	
	NC	131	132	NC	
	NC	133	134	NC	

	3.3V	135	136	12V	
	NC	137	138	NC	
	NC	139	140	NC	
	3.3V	141	142	12V	
	NC	143	144	NC	
	NC	145	146	NC	
	3.3V	147	148	12V	
	NC	149	150	NC	
	NC	151	152	NC	
	3.3V	153	154	12V	
	NC	155	156	NC	
	NC	157	158	NC	
	3.3V	159	160	Presence LED*	

Notes:

‡ New pins on REV D of PCB

* Connect to GND to turn LED on.

Connector J4, LVDS

J4 is the third HSMC connector is located at the top of the board. It provides 96 I/Os routed as 48 differential pairs. This connector also includes two dedicated differential clocks connected to PLL1.

The Cyclone III differential signal pairs are capable of being configured as either receivers or transmitters. To allow greater flexibility, the ViClaro III does not include differential terminations. All pairs used as inputs must be terminated on the daughter board as shown below. Moving the termination resistors from the baseboard to the daughter board allows a wide variety of input and output configurations because the direction of each pair is not fixed. A simple change in the daughter board can provide an entirely new arrangement of input and output.

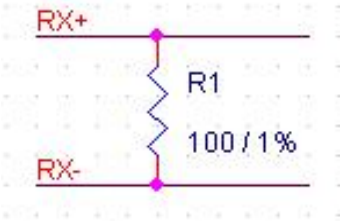

Figure 4 - LVDS Receive Termination

When routing an LVDS daughter board, place the receive termination resistors as close to the HSMC connector as possible.

The LVDS pins are located in banks 1 and 2. These banks are powered at 2.5V. LVDS I/O pins should be configured with the LVDS I/O standard. It is also possible to use the LVDS pins as single-ended I/O. In this case they should be configured with the 2.5V I/O standard.

Table 14: J4, LVDS (HSMC connector) pin assignments

Cyclone III Pin #	Signal Name	HSMC Pin #	HSMC Pin #	Signal Name	Cyclone III Pin #
	NC	1	2	NC	
	NC	3	4	NC	
	NC	5	6	NC	
	NC	7	8	NC	
AE3	LVDS_p45	9	10	LVDS_p47	AE2
AF2	LVDS_n45	11	12	LVDS_n47	AE1
AC3	LVDS_p43	13	14	LVDS_p46	AD2
AD3	LVDS_n43	15	16	LVDS_n46	AD1
AC5	LVDS_p41	17	18	LVDS_p44	AC2
AC4	LVDS_n41	19	20	LVDS_n44	AC1
AB6	LVDS_p39	21	22	LVDS_p42	AB2
AB5	LVDS_n39	23	24	LVDS_n42	AB1
AA6	LVDS_p37	25	26	LVDS_p40	AA4
AA5	LVDS_n37	27	28	LVDS_n40	AA3
Y6	LVDS_p35	29	30	LVDS_p38	Y4
Y5	LVDS_n35	31	32	LVDS_n38	Y3
Y10	I2C_SDA	33	34	I2C_SCL	AA10
	NC	35	36	NC	
	NC	37	38	NC	
	NC	39	40	NC	
T8	LVDS_D0	41	42	LVDS_D1	T7
M5	LVDS_D2	43	44	LVDS_D3	L5
	3.3V	45	46	12V	
W8	LVDS_p33	47	48	LVDS_p36	W2
Y7	LVDS_n33	49	50	LVDS_n36	W1
	3.3V	51	52	12V	
V8	LVDS_p31	53	54	LVDS_p34	W4
V7	LVDS_n31	55	56	LVDS_n34	W3

	3.3V	57	58	12V	
V6	LVDS_p29	59	60	LVDS_p32	V4
V5	LVDS_n29	61	62	LVDS_n32	V3
	3.3V	63	64	12V	
U6	LVDS_p27	65	66	LVDS_p30	V2
U5	LVDS_n27	67	68	LVDS_n30	V1
	3.3V	69	70	12V	
R7	LVDS_p25	71	72	LVDS_p28	U2
R6	LVDS_n25	73	74	LVDS_n28	U1
	3.3V	75	76	12V	
M8	LVDS_p23	77	78	LVDS_p26	U3
M7	LVDS_n23	79	80	LVDS_n26	U4
	3.3V	81	82	12V	
K8	LVDS_p21	83	84	LVDS_p24	T4
L8	LVDS_n21	85	86	LVDS_n24	T3
	3.3V	87	88	12V	
J7	LVDS_p19	89	90	LVDS_p22	R2
K7	LVDS_n19	91	92	LVDS_n22	R1
	3.3V	93	94	12V	
R3	LVDS_p20	95	96	LVDS_CLKIN_p1	Y2
R4	LVDS_n20	97	98	LVDS_CLKIN_n1	Y1
	3.3V	99	100	12V	
M4	LVDS_p17	101	102	LVDS_p18	L4
M3	LVDS_n17	103	104	LVDS_n18	L3
	3.3V	105	106	12V	
P2	LVDS_p15	107	108	LVDS_p16	L2
P1	LVDS_n15	109	110	LVDS_n16	L1
	3.3V	111	112	12V	
N4	LVDS_p13	113	114	LVDS_p14	K4
N3	LVDS_n13	115	116	LVDS_n14	K3
	3.3V	117	118	12V	
L7	LVDS_p11	119	120	LVDS_p12	K2
L6	LVDS_n11	121	122	LVDS_n12	K1
	3.3V	123	124	12V	
J6	LVDS_p9	125	126	LVDS_p10	J4

J5	LVDS_n9	127	128	LVDS_n10	J3
	3.3V	129	130	12V	
M2	LVDS_p7	131	132	LVDS_p8	H4
M1	LVDS_n7	133	134	LVDS_n8	H3
	3.3V	135	136	12V	
G6	LVDS_p5	137	138	LVDS_p6	G2
G5	LVDS_n5	139	140	LVDS_n6	G1
	3.3V	141	142	12V	
G4	LVDS_p3	143	144	LVDS_p4	F2
G3	LVDS_n3	145	146	LVDS_n4	F1
	3.3V	147	148	12V	
D2	LVDS_p1	149	150	LVDS_p2	E3
D1	LVDS_n1	151	152	LVDS_n2	F3
	3.3V	153	154	12V	
D3	LVDS_p0	155	156	LVDS_CLKIN_p2	J2
C2	LVDS_n0	157	158	LVDS_CLKIN_n2	J1
	3.3V	159	160	Presence LED*	

* Note: Connect to GND to turn LED on.

USB 2.0 PHY

Included on the ViClaro III is an NXP ISP1506A ULPI high-speed USB on-the-go transceiver (U20). The USB interface pins are located in bank 3. These banks are powered at 2.5 volts and use the 2.5V I/O standard. For more information see the NXP ISP1506A datasheet.

Table 15: Cyclone III – USB pin assignments

Signal Name	Pin Number
USB_CLOCK	AH15
USB_DATA0	AG3
USB_DATA1	AG4
USB_DATA2	AF3
USB_DATA3	AF4
USB_STP	AH3
USB_DIR	AE4
USB_NXT	AH4
USB_RESET_N	AD4

EEPROM – SHA-1 Engine

U11 is the DS28E01-100 EEPROM that supports challenge and response security authentication engine. (This feature was added in Rev D of the PCB.) The security is implemented with the ISO/IEC 10118-3 Secure Hash Algorithm (SHA-1). The device can process SHA-1 input block secrets of 64-bits and 320-bits in conjunction with a 40-bit random challenge and additional device data to provide a high degree of authentication security between a host system and slave accessories. The EEPROM interface pins are located in bank 3. These banks are powered at 2.5 volts and use the 2.5V I/O standard. For more information see the DS28E01-100 datasheet and the Altera website for application notes and white papers:

(http://www.altera.com/support/refdesigns/sys-sol/indust_mil/ref-des-secur-mem.html).

Table 16: EEPROM – SHA-1 Engine

Signal Name	Pin Number
SHA1	Y11

LVDS Daughter Board

Included with the ViClaro III is an LVDS daughter board. It is designed for use with HSMC header J4 on the top edge of the ViClaro III. The LVDS board contains four Hirose DF13-40DP-1.25V connectors; two for transmit and two for receive. Each connector provides two links of five channels each. Each connector provides two clocks, one for each link (only one receive clock per connector supported by ViClaro III due to PLL requirements). The LVDS daughter board comes with two 40-pin straight-through cables.

The Tables below provide the pin out for the LVDS Daughter Board. An arrow on the side of each connector indicates pin 1.

For more information on interfacing to LVDS panels, refer to the VESA Standards available on the web.

Table 17: J4, LVDS Daughter Card – J2 pin assignments

Cyclone III Pin #	Signal Name	HSMC Pin #	HSMC Pin #	Signal Name	Cyclone III Pin #
	NC	1	2	NC	
	GND	3	4	GND	
AD2	RXA_p0	5	6	RXB_p0	AC2
AD1	RXA_n0	7	8	RXB_n0	AC1
	GND	9	10	GND	
AB2	RXA_p1	11	12	RXB_p1	AA4
AB1	RXA_n1	13	14	RXB_n1	AA3
	GND	15	16	GND	
Y4	RXA_p2	17	18	RXB_p2	W2
Y3	RXA_n2	19	20	RXB_n2	W1
	GND	21	22	GND	
W4	RXA_p3	23	24	RXB_p3	V4
W3	RXA_n3	25	26	RXB_n3	V3
	GND	27	28	GND	
V2	RXA_p4	29	30	RXB_p4	U2
V1	RXA_n4	31	32	RXB_n4	U1
	GND	33	34	GND	
U3	RXA_p5	35	36	RXB_p5 (clk_p)	Y2
U4	RXA_n5	37	38	RXB_n5 (clk_n)	Y1
	GND	39	40	GND	

Table 18: J4, LVDS Daughter Card – J4 pin assignments

Cyclone III Pin #	Signal Name	HSMC Pin #	HSMC Pin #	Signal Name	Cyclone III Pin #
	NC	1	2	NC	
	GND	3	4	GND	
R2	RXC_p0	5	6	RXD_p0	T4
R1	RXC_n0	7	8	RXD_n0	T3
	GND	9	10	GND	
L4	RXC_p1	11	12	RXD_p1	L2
L3	RXC_n1	13	14	RXD_n1	L1
	GND	15	16	GND	
K4	RXC_p2	17	18	RXD_p2	K2
K3	RXC_n2	19	20	RXD_n2	K1
	GND	21	22	GND	
J4	RXC_p3	23	24	RXD_p3	H4
J3	RXC_n3	25	26	RXD_n3	H3
	GND	27	28	GND	
G2	RXC_p4	29	30	RXD_p4	F2
G1	RXC_n4	31	32	RXD_n4	F1
	GND	33	34	GND	
E3	RXC_p5	35	36	RXD_p5 (clk_p)	J2
F3	RXC_n5	37	38	RXD_n5 (clk_n)	J1
	GND	39	40	GND	

Table 19: J4, LVDS Daughter Card – J3 pin assignments

Cyclone III Pin #	Signal Name	HSMC Pin #	HSMC Pin #	Signal Name	Cyclone III Pin #
	NC	1	2	NC	
	GND	3	4	GND	
AE2	TXA_p0	5	6	TXB_p0	AE3
AE1	TXA_n0	7	8	TXB_n0	AF2
	GND	9	10	GND	
AC3	TXA_p1	11	12	TXB_p1	AC5
AD3	TXA_n1	13	14	TXB_n1	AC4
	GND	15	16	GND	
AB6	TXA_p2	17	18	TXB_p2	AA6
AB5	TXA_n2	19	20	TXB_n2	AA5
	GND	21	22	GND	
Y6	TXA_p3	23	24	TXB_p3	W8
Y5	TXA_n3	25	26	TXB_n3	Y7
	GND	27	28	GND	
V8	TXA_p4	29	30	TXB_p4	V6
V7	TXA_n4	31	32	TXB_n4	V5
	GND	33	34	GND	
U6	TXA_p5 (clk_p)	35	36	TXB_p5 (clk_p)	R7
U5	TXA_n5 (clk_n)	37	38	TXB_n5 (clk_n)	R6
	GND	39	40	GND	

Table 20: J4, LVDS Daughter Card – J5 pin assignments

Cyclone III Pin #	Signal Name	HSMC Pin #	HSMC Pin #	Signal Name	Cyclone III Pin #
	NC	1	2	NC	
	GND	3	4	GND	
M8	TXC_p0	5	6	TXD_p0	K8
M7	TXC_n0	7	8	TXD_n0	L8
	GND	9	10	GND	
J7	TXC_p1	11	12	TXD_p1	M4
K7	TXC_n1	13	14	TXD_n1	M3
	GND	15	16	GND	
P2	TXC_p2	17	18	TXD_p2	N4
P1	TXC_n2	19	20	TXD_n2	N3
	GND	21	22	GND	
L7	TXC_p3	23	24	TXD_p3	J6
L6	TXC_n3	25	26	TXD_n3	J5
	GND	27	28	GND	
M2	TXC_p4	29	30	TXD_p4	G6
M1	TXC_n4	31	32	TXD_n4	G5
	GND	33	34	GND	
G4	TXC_p5	35	36	TXD_p5 (clk_p)	D2
G3	TXC_n5	37	38	TXD_n5 (clk_n)	D1
	GND	39	40	GND	

Digital Video Receiver / Transmitter Board

Included with the ViClaro III is either a Microtronix HDMI Receiver / Transmitter daughter board or a Bitec DVI Receiver / Transmitter daughter board. When acting as a video receiver, these boards may be installed on any HSMC header. The transmit function is only supported on HSMC header J4. The reference designs that incorporate video output require the use of this card and installed on header J4.

For the DVI board, the user is referred to the Bitec corporate website http://www.bitec.ltd.uk/index.html for additional reference designs and documentation.

HDMI Receiver / Transmitter Board

The Microtronix HDMI Receiver / Transmitter Daughter Card interfaces a HDMI receiver and transmitter to your Altera FPGA development kit using the HSMC expansion connector. The receiver also supports an analog component video (YCbCr) interface.

The card uses the Analog Device AD9889 HDMI v1.1 transmitter to support HDTV formats up to 1080i at 60 Hz. Using an 80 MHz, high-definition multimedia interface (HDMI 1.1) transmitter. With the inclusion of HDCP a encryption key, the AD9889 allows the secure transmission of protected content as specified by the HDCP 1.1 protocol.

The AD9880 HDMI Receiver offers designers the flexibility of an analog interface and digital high definition multimedia interface (HDMI) v1.1 receiver integrated on a single chip. The receiver supports resolutions to 1080p at 60 Hz.

The cards can support high band-width digital content protection (HDCP) when programmed with a HDCP encryption key.

The Microtronix HDMI Receiver / Transmitter Daughter Card is supplied with HD a pass-through reference design for the Altera Cyclone III Starter Kit and the Microtronix ViClaro III HD Display Panel - Video IP Dev Kit.

ViClaro III Software Installation

The ViClaro III software requires an installed version of the Altera Quartus II version 7.2 FPGA design software (either the Altera Web Edition or the Full Edition).

The ViClaro III software is supplied by Microtronix on a CD or as a zipped file. If you received the latter, unzip the file to a temporary file directory and run the setup.exe file. The software should self-install from the CD or it can be manually installed by running the setup.exe file.

WARNING: Remove older installations of the ViClaro III software from the PC prior to installing the new version of software.

ViClaro III Factory Default Configuration

The ViClaro III Kit is shipped with a factory default configuration project programmed into the flash configuration device. This project dynamically scales progressive input video to 1080p at 60 Hz. (50 Hz is shipped to Europe.)

This is supplied as a SOF file under

DVI Rx/Tx Board:

`example/dvi/vip_dynamic_scaler_1080p` and named `vip_dynamic_scaler_1080p.sof`.

HDMI Rx/Tx Board:

`example/dvi/vip_dynamic_scaler_1080p` and named `vip_dynamic_scaler_1080p.sof`.

NOTE: The default project will only work with the supplied daughter board (DVI or HDMI).

Connecting the Cables

1. Remove the ViClaro III board from its protective ESD bag.
   NOTE: Use good ESD practices to avoid electrically damaging the boards.
2. Mount the ***HSMC DVI Rx/Tx Board*** or ***HDMI Rx/Tx Board*** on J4 using the supplied mounting hardware.
3. Power the AC-DC 12V adapter and connect to J7.
4. Connect the Altera USB Blaster JTAG cable to J1 on the ViClaro III and a USB port on the PC/laptop.
5. Connect the DVI or HDMI output from the TX port on the respective daughter board to the auxiliary display monitor.

Running the Default Configuration

The default configuration demonstrates the basic operation of the board. The following steps are required:

1. Apply power to the board.
2. The Cyclone III will load the default program configuration from flash memory.
3. Apply a progressive (480p, 720p, 1080p) video input. The project will scale the input video and display it at 1080p.

Running Video Reference Designs

The ViClaro III Kit includes a number of pre-compiled Quartus reference designs to demonstrate the functionality of the board.

The designs are supplied as pre-compiled SOF files and also as Quartus design files with the full source. The SOF files can be run by downloading them through the JTAG port into the Cyclone III FPGA on the board.

NOTE: An Altera USB-Blaster cable is required to load SOF program files onto the ViClaro III board.

Configure USB-Blaster

This step is required if the USB-Blaster has not yet been configured to work with the Quartus software.

1. Connect the USB-Blaster to the JTAG port of the ViClaro III board being careful to align the pin numbers.
2. Plug the other end of the cable into the PC/Laptop.
3. Start Quartus.

4. Connect to the JTAG programmer by selecting > Tools > Programmer > Hardware.
    a. Click on Hardware Setup box. Confirm/select USB-Blaster.
    b. Click on Auto Detect box. This will find the programmable devices on the ViClaro III board.

NOTE: To load SOF or POF files into the FPGA or flash memory, refer to Appendix A and B respectively.

Overview of Reference Designs

The ViClaro III reference designs are supplied as pre-compiled SOF files and as Quartus design files with the full source. The DVI/HDMI based designs require a variety of video sources and a monitor with a DVI or HDMI input supporting resolutions of 720p and 1080p 50/59.94/60Hz. The DVI/HDMI-to-LVDS Video display reference design requires a Samsung LN-T4071F television and custom LVDS cables. This design is supplied as a frame of reference only.

The designs are listed in the following table.

Table 21: Quartus Reference Designs

Description	Directory & Filename
480i to 720p deinterlacer and scaler @ 60 Hz	DVI reference design: example/dvi/vip_deinterlace_480i_720p/ vip_deinterlace_480i_720p.sof HDMI reference design: example/hdmi/vip_deinterlace_480i_720p/ vip_deinterlace_480i_720p.sof
480i to 720p deinterlacer and scaler @ 50 Hz	DVI reference design: example/dvi/50Hz/vip_deinterlace_480i_720p/ vip_deinterlace_480i_720p.sof HDMI reference design: example/hdmi/50Hz/vip_deinterlace_480i_720p/ vip_deinterlace_480i_720p.sof
1080i to 1080p deinterlacer @ 60 Hz	DVI reference design: example/dvi/vip_deinterlace_1080i_1080p/ vip_deinterlace_1080i_1080p.sof HDMI reference design: example/hdmi/vip_deinterlace_1080i_1080p/ vip_deinterlace_1080i_1080p.sof
1080i to 1080p deinterlacer @ 50 Hz	DVI reference design: example/dvi/50Hz/vip_deinterlace_1080i_1080p/ vip_deinterlace_1080i_1080p.sof HDMI reference design: example/hdmi/50Hz/vip_deinterlace_1080i_1080p/ vip_deinterlace_1080i_1080p.sof

Dynamic scaler to 1080p @ 60 Hz.	DVI reference design: example/dvi/vip_dynamic_scaler_1080p/ vip_dynamic_scaler_1080p.sof HDMI reference design: example/hdmi/vip_dynamic_scaler_1080p/ vip_dynamic_scaler_1080p.sof
Dynamic scaler to 1080p @ 50 Hz.	DVI reference design: example/dvi/50Hz/vip_dynamic_scaler_1080p/ vip_dynamic_scaler_1080p.sof HDMI reference design: example/hdmi/50Hz/vip_dynamic_scaler_1080p/ vip_dynamic_scaler_1080p.sof
720p logo overlay @ 60 Hz.	DVI reference design: example/dvi/vip_mixer_720p/ vip_mixer_720p.sof HDMI reference design: example/hdmi/vip_mixer_720p/ vip_mixer_720p.sof
720p logo overlay @ 50 Hz.	DVI reference design: example/dvi/50Hz/vip_mixer_720p/ vip_mixer_720p.sof HDMI reference design: example/hdmi/50Hz/vip_mixer_720p/ vip_mixer_720p.sof
HDMI/DVI 1080p capture & LVDS display	DVI reference design: example/dvi/hd_frame_capture_lvds/qdesign/ hd_frame_capture.sof HDMI reference design: example/hdmi/hd_frame_capture_lvds/qdesign/ hd_frame_capture.sof
LVDS Pass-through	example/viclaroiii_lvds/ lvds_top.sof

Microtronix IP Cores

The ViClaro III reference designs incorporate the Microtronix Streaming and Avalon Multi-port DDR2 SDRAM Memory Controllers, the Microtronix I^2C Master / Slave / PIO Controller, and the Video LVDS SerDes Transmitter / Receiver IP Cores.

The ViClaro III Kit purchase includes the following IP Core licenses:

- A full 1-year license for the LVDS core.
- A full 1-year license for the Avalon Multi-port DDR2 SDRAM Memory Controller
- A full 1-year license for the I^2C Master / Slave /PIO Controller
- Extended OpenCore Plus licenses of the following IP:

- Streaming Multi-port SDRAM Memory Controller

To receive your IP core license contact sales sales@microtronix.com and provide them with the serial number of your board. These licenses are required if you are to recompile or develop new IP core designs.

Block Diagrams

480i to 720p Deinterlacer and Scaler

The following diagram provides an overview of the IP blocks required for the deinterlacer and scaler design. Pressing pushbutton SW1 resets the Nios II processor.

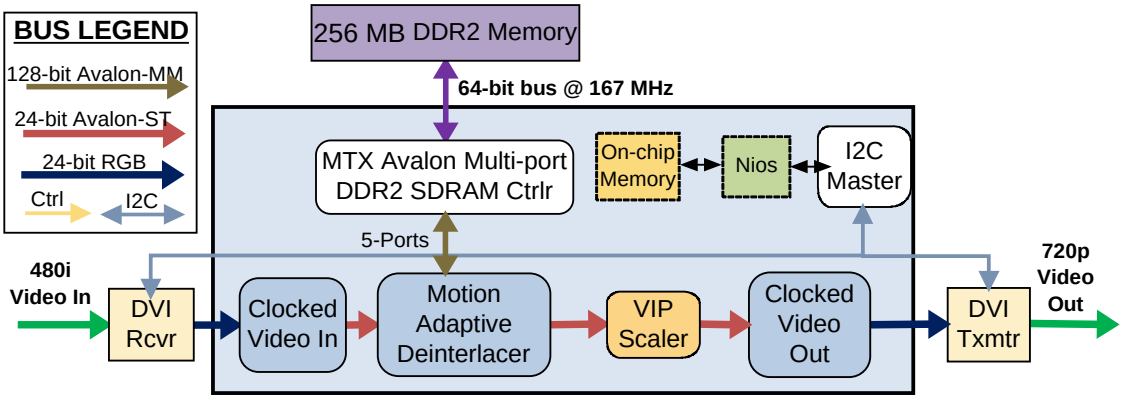

Figure 5: Block Diagram of HD Deinterlacer/Scaler System

PLL Clock Domains

The DDR2 memory uses one PLL running at 167MHz. The DVI/HDMI transmitter uses one PLL running at 74.25MHz. The entire SOPC Builder system operates from another PLL running at 100MHz.

Avalon Multi-port DDR2 SDRAM Memory Controller

The Avalon Multi-port DDR2 SDRAM Memory controller interfaces to the DDR2 using a 64-bit data bus.

Altera VIP Suite

This design uses the Clocked Video Input and Clocked Video Output to interface to the DVI/HDMI transmitter and receiver. The Deinterlacer component is used in Motion Adaptive mode to convert the incoming 480i video to 480p. The Scaler increases the 480p video to 720p using the Bicubic algorithm.

DVI/HDMI Receiver/Transmitter

The data interfaces are 24-bits wide to the receiver and transmitter. These IC's are configured by an I^2C master controller by software running on the Nios II processor.

1080i to 1080p Deinterlacer

The following diagram provides an overview of the IP blocks required for the deinterlacer design. Pressing pushbutton SW1 resets the Nios II processor.

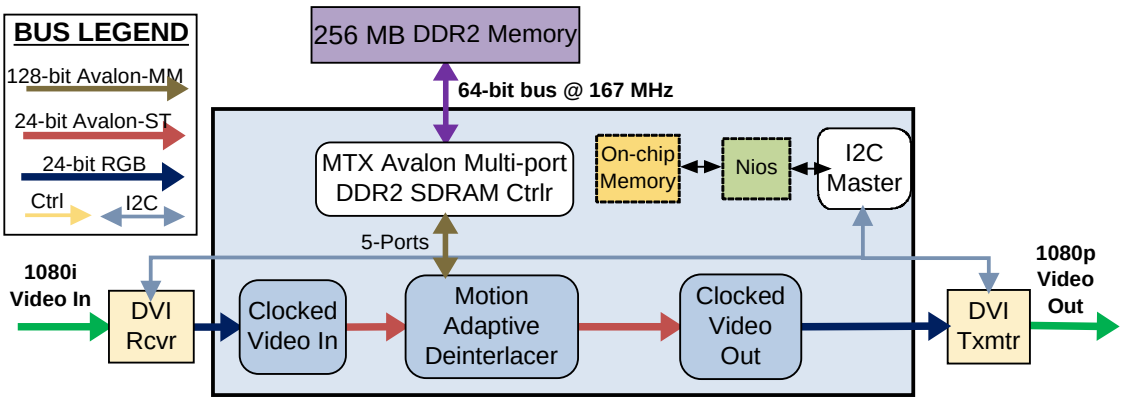

Figure 6: Block Diagram of HD Deinterlacer System

PLL Clock Domains

The DDR2 memory uses one PLL running at 167MHz. The DVI/HDMI transmitter uses one PLL running at 148.5MHz. The SOPC Builder system operates from another PLL with two outputs. The Nios II processor and peripherals run at 81MHz while the video IP runs at 135MHz.

Avalon Multi-port DDR2 SDRAM Memory Controller

The Avalon Multi-port DDR2 SDRAM Memory controller interfaces to the DDR2 using a 64-bit data bus.

Altera VIP Suite

This design uses the Clocked Video Input and Clocked Video Output to interface to the DVI/HDMI transmitter and receiver. The Deinterlacer component is used in Motion Adaptive mode to convert the incoming 1080i video to 1080p.

DVI/HDMI Receiver/Transmitter

The data interfaces are 24-bits wide to the receiver and transmitter. These IC's are configured by an I^2C master controller by software running on the Nios II processor.

Dynamic Scaler to 1080p

The following diagram provides an overview of the IP blocks required for the dynamic scaler design. Pressing pushbutton SW1 resets the Nios II processor.

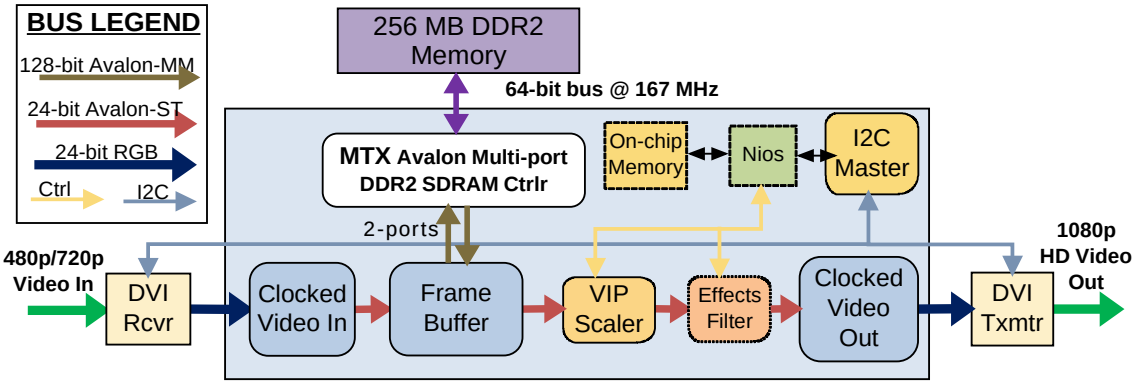

Figure 7: Block Diagram of HD Dynamic Scaler System

PLL Clock Domains

The DDR2 memory uses one PLL running at 167MHz. The DVI/HDMI transmitter uses one PLL running at 148.5MHz. The SOPC Builder system operates from another PLL with two outputs. The Nios II processor and peripherals run at 27MHz while the video IP runs at 135MHz.

Avalon Multi-port DDR2 SDRAM Memory Controller

The Avalon Multi-port DDR2 SDRAM Memory controller interfaces to the DDR2 using a 64-bit data bus.

Altera VIP Suite

This design uses the Clocked Video Input and Clocked Video Output to interface to the DVI/HDMI transmitter and receiver. The Frame Buffer is used in triple-buffer mode to convert between the input and output frame rates. The Scaler dynamically converts incoming progressive video to 1080p using the Bilinear algorithm.

DVI/HDMI Receiver/Transmitter

The data interfaces are 24-bits wide to the receiver and transmitter. These IC's are configured by an I^2C master controller by software running on the Nios II processor.

Effects Filter

Pressing SW2 cycles through a number of output color effects. These are listed below:

- No effect
- Red only
- Green only
- Blue only
- Reverse video

720p Logo Overlay

The following diagram provides an overview of the IP blocks required for the mixer design. Pressing pushbutton SW1 resets the Nios II processor.

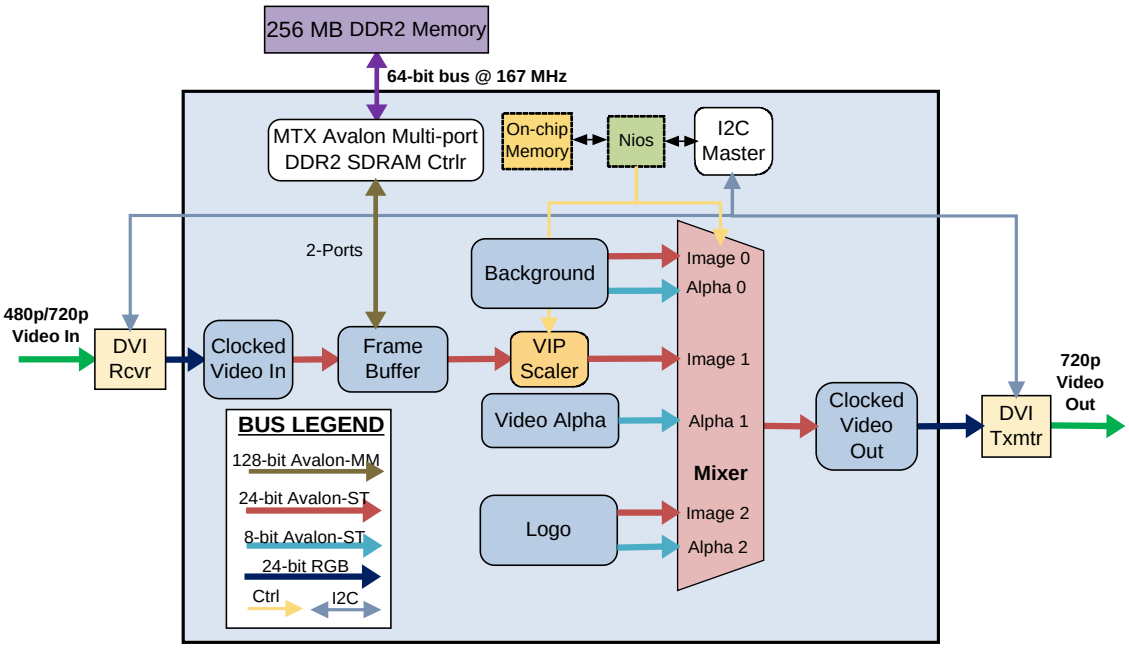

Figure 8: Block Diagram of HD Mixer System

PLL Clock Domains

The DDR2 memory uses one PLL running at 167MHz. The DVI/HDMI transmitter uses one PLL running at 74.25MHz. The SOPC Builder system operates from another PLL with two outputs. The Nios II processor and peripherals run at 54MHz while the video IP runs at 108MHz.

Avalon Multi-port DDR2 SDRAM Memory Controller

The Avalon Multi-port DDR2 SDRAM Memory controller interfaces to the DDR2 using a 64-bit data bus.

ALTERA VIP SUITE

This design uses the Clocked Video Input and Clocked Video Output to interface to the DVI/HDMI transmitter and receiver. The Frame Buffer is used in triple-buffer mode to convert between the input and output frame rates. The Scaler dynamically converts incoming progressive video to 720p using the Bilinear algorithm. Finally, the Mixer combines the background layer with the scaled video and the logo overlay to create the desired output.

CUSTOM VIDEO COMPONENTS

Three of custom video components were created for this design. The 720p Background component contains two Avalon-ST sources: a black 24-bit 720p background image, and an opaque 8-bit 720p alpha channel. The 720p Alpha Channel contains a single Avalon-ST source: am opaque 8-bit 720p alpha channel. The Microtronix Logo component contains two Avalon-ST sources: a 24-bit color image source and an 8-bit alpha source. The data for both logo sources is read from on-chip ROM.

DVI/HDMI RECEIVER/TRANSMITTER

The data interfaces are 24-bits wide to the receiver and transmitter. These IC's are configured by an I^2C master controller by software running on the Nios II processor.

HD Frame Capture – DVI/HDMI-LVDS

This project takes a 1080p DVI/HDMI input signal and displays the output on a LVDS panel. The supplied design uses a Samsung LTA400HH-LH1 display panel found in a 1080p 120 Hz HDTV.

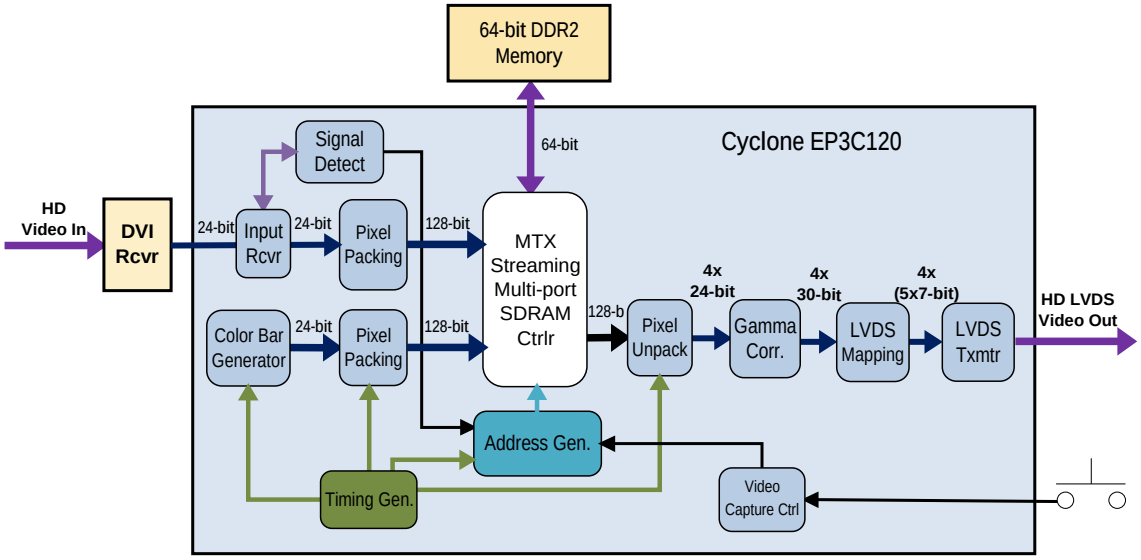

Figure 9: DVI – LVDS Video Pass-through & Capture

GAMMA CORRECTION

This block expands data from 24-bit to 30-bits and provides gamma correction as required by an LCD panel when driven using an LVDS interface,

LVDS MAPPING

The LVDS interface uses the Microtronix LVDS IP Core. The mapping block puts the data in the correct bit position and channel required by the LVDS panel. This block maps the 4 channels of 30-bit parallel data into 4 links of 5 data channels of 7-bits.

LVDS TRANSMITTER

The LVDS Transmitter converts 35 bits of parallel data into 5 LVDS data streams and one LVDS clock stream. The data is clocked at 7 times the rate of the LVDS Tx clock.

NOTE: For more information on the Microtronix LVDS SerDes Transmitter/Receiver IP core refer to the user documentation supplied with the core.

Configuring HD EDID for Correct Refresh Rate

Before running the DVI or HDMI based reference designs, it is first necessary to program the Cyclone III EP3C120 device on the ViClaro III to configure the EDID EEPROM device on the (Bitec) HSMC DVI Rx/Tx board (or HDMI Rx/Tx board) to make the transmitter operate at either a 50 or 60 Hz refresh rate. These SOF files can also be used to verify correct operation of the video source and display as they pass video directly from input to output.

1. From within Quartus, under the **Tools** menu, open **Programmer.** i.e. > Tools > Programmer
2. Click Auto Detect.
3. Browse to the location of the ***Bitec_EDID_50.sof*** (50 Hz) or the ***Bitec_EDID_60.sof*** (60 Hz) EDID programming file (under the example directory). If using the HDMI board then the file names are ***hdmi_EDID_50.sof*** and ***hdmi_EDID_60.sof*** for 50Hz and 60Hz refresh rates respectively. Select the appropriate file for the refresh rate of your auxiliary monitor. It will be located in the directory where the files were extracted.
4. Select/highlight the appropriate file > Open. The file will be listed under the file column of the EP3C120 device.
5. Click the check box under the Program / Configure column.
6. Click on the Start box to program the device. The LED9 labeled CONF DONE will turn amber when the Cyclone III device has programmed and configured the EDID device on the **DVI or HDMI Rx/TX Board**. The ViClaro III system is now programmed to pass incoming video to the output port to verify the PC is configured correctly.
7. Connect the cable from the second DVI/HDMI video port of the PC system to the RX port of the HSMC DVI or HDMI Rx/Tx board.

It is now possible to load the ViClaro III board with one of the DVI based reference designs.

Running ViClaro III Reference Designs

The Dynamic Scaler reference design can operate at a resolution of 480p, 720p, or 1080p (as detected from the EDID on the DVI/HDMI cable connected to the auxiliary monitor.)

WARNING: *Make sure there is no DVI/HDMI cable from the laptop/PC to the ViClaro III board until the ViClaro III board is fully programmed and operational.*

8. From within Quartus, under the **Tools** menu, open **Programmer.** i.e. > Tools > Programmer
9. Click Auto Detect.
10. Select the EP3C120 from the three items listed. Right click > Change File.
11. Browse to the location of the ***vip_dynamic_scaler_1080p.sof*** programming file. Select the appropriate file for the matching the refresh rate of your auxiliary monitor. It will be located in the directory where the files were extracted.

12. Select/highlight the file > Open. The file will be listed under the file column of the EP3C120 device.
13. Click the check box under the Program / Configure column.
14. Click on the Start box to program the device. The LED9 labeled CONF DONE will turn amber when the Cyclone III device is programmed and running.
15. Connect the DVI or HDMI cable from the display monitor to the TX connector on the DVI or HDMI Board. The board will scale progressive input video to 1080p.

Importing Software

All of the SOPC Builder based example designs include software to configure the hardware. These software projects can be imported into the Nios II IDE to be recompiled or modified.

1. From within Nios II IDE, under the **File** menu, select **Import.**
2. Select Altera Nios II -> Existing Nios II IDE project into workspace, click **Next**.
3. Browse to the ***software*** directory of the example design of interest. There will be two subdirectories, the import process must be repeated for each (e.g. mixer_hdmi, mixer_hdmi_syslib).
4. Select one of the subdirectories under ***software*** and click **OK**.
5. Click **Finish** to start the import.
6. A dialog may appear asking to remove the Release and/or Debug directories, click **Yes**.
7. Repeat for this process for the second subdirectory under ***software***.

Appendix A: Loading Designs into the FPGA

The following procedure can be used to load a SOF file to the FPGA through JTAG. These steps require the board to be powered and connected to the PC through a JTAG cable (USB-Blaster, etc).

1. Start Quartus.
2. From the **Tools** menu, select **Programmer**.
3. Click **Auto Detect**.
4. Select the line with the **EP3C120** device.
5. Click **Change File** and browse to the SOF file (reference design) you wish to load.
6. Check the **Program/Configure** box.
7. Click **Start** to program the FPGA.

WARNING: The factory default configuration is initially stored the flash memory device. If the flash device is erased (empty) and SW3 is pressed to reconfigure, the FPGA will go into an unusable state and the ViClaro III board will need to be power cycled.

Appendix B: Loading Designs into the On-Board Flash

Designs can be loaded into the on-board flash to configure the FPGA on power-up. Below is the procedure for programming the flash through the JTAG.

Converting a SOF File to a POF for the Flash Device

The SOF file generated by Quartus II must be converted to a POF file for flash programming.

1. Open your Quartus project.
2. From the **File** menu, select **Convert Programming Files**.
3. Select **Programmer Object File (.pof)** from the **Programming file type** list. The default file name will be output_file.pof.
4. Select **CFI_128MB** as the configuration device and **1-bit Passive Serial** as the mode. Click **Options** and enter 0x00FE0000 as the option bit address.
5. Select **SOF Data** under **Input files to convert**. Click **Add File** and browse to the SOF file you would like to convert.
6. Select the SOF file under **Input files to convert** and click **Properties** if you wish to enable compression.
7. Click **OK** to generate the POF.

Programming the Flash Device

The following procedure can be used to load a converted POF file to the flash device through JTAG. These steps require the board to be powered and connected to the PC through a JTAG cable (USB-Blaster, etc).

1. From the **Tools** menu, select **Programmer**.
2. Click **Auto Detect**.
3. Select the line with the **CFI_128MB** device.
4. Click **Change File** and browse to the POF file created with the programming file converter.
5. Check the **Program/Configure** box.
6. Click **Start** to program the flash.

Appendix C: Testing PCIe Functionality

If you did not install the PciExpress test software when installing the ViClaro III software, locate the Install CD and browse to **PciExpress** and run the setup.exe program. This test program is only known to work under Windows XP. There may be issues under 2000 or Vista.

The ViClaro must be programmed with the ViClaroIII_PCIe_Demo.sof file (in \example\pcie\) when the PC is powered up. The PC should be reset once this is done in order to properly recognize the card. You may wish to enter the PC's BIOS setup screen or otherwise pause the boot-up while programming the card. You may also convert the .sof file to a .pof to program the flash memory if desired (see Appendix B: Loading Designs into the On-Board Flash).

The PCI Express core IP is provided by NorthWest Logic and can therefore only be distributed in a binary .sof file. Please contact Microtronix if you are interested in licensing this IP to use in your design.

The PciExpress program allows you to examine the PCI configuration, perform memory and throughput tests, and “PEEK” and “POKE” memory and register space.

In this demo, memory is accessed via BAR1, and consists of 8KB of on-chip RAM

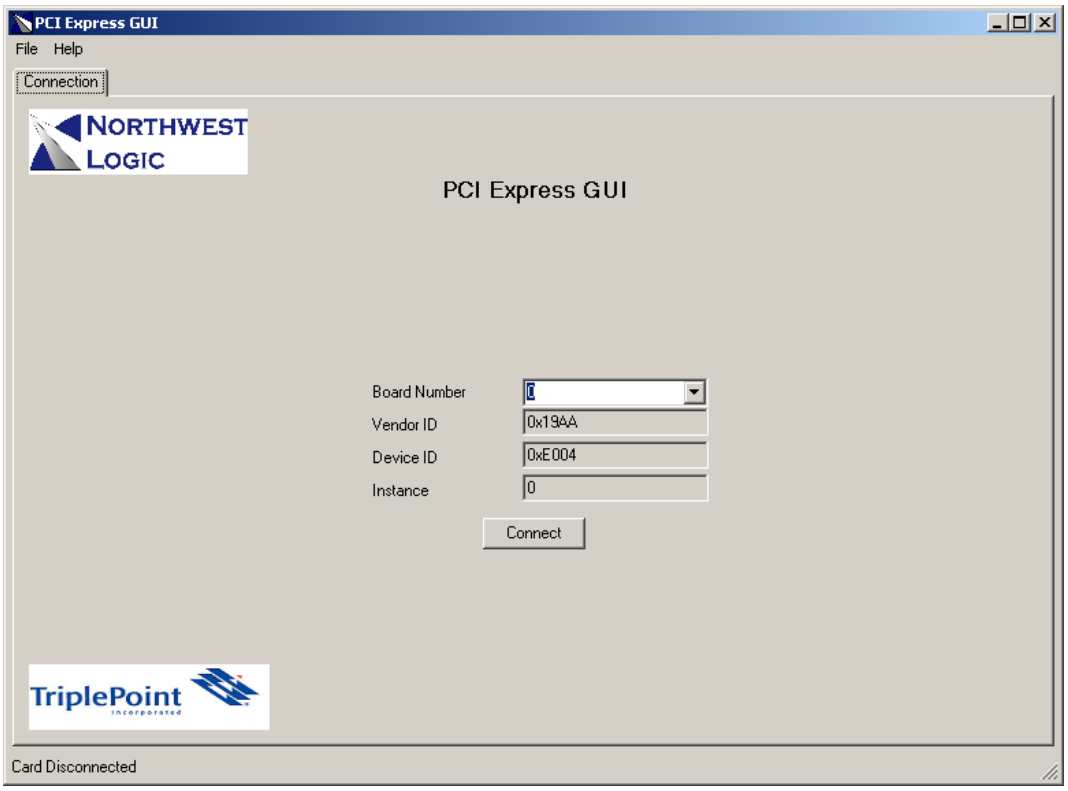

Figure 10: PciExpress GUI

When you press **Connect,** the four other tabs will become available (Figure 11: PciExpress – Memory Access Page). Try experimenting with the **Self Test** (use BAR1) and the **Throughput Graph**. (Note that the **Explain Results** button is non-functional, as is the **Help** menu.)

Microtronix has seen currently unexplained results in the throughput test using different motherboards. For example, two Asus motherboards using the same chip “set” provided widely different numbers. One showed a maximum DMA throughput of 690MB/s – about right for four lanes of PCIe. The other performed at a poor 310MB/s. Though both boards used the nVidia nForce 590 SLI MCP chip, only the Asus *Crosshair* provided the good performance noted above. We currently therefore cannot predict which boards will perform well and which won't.

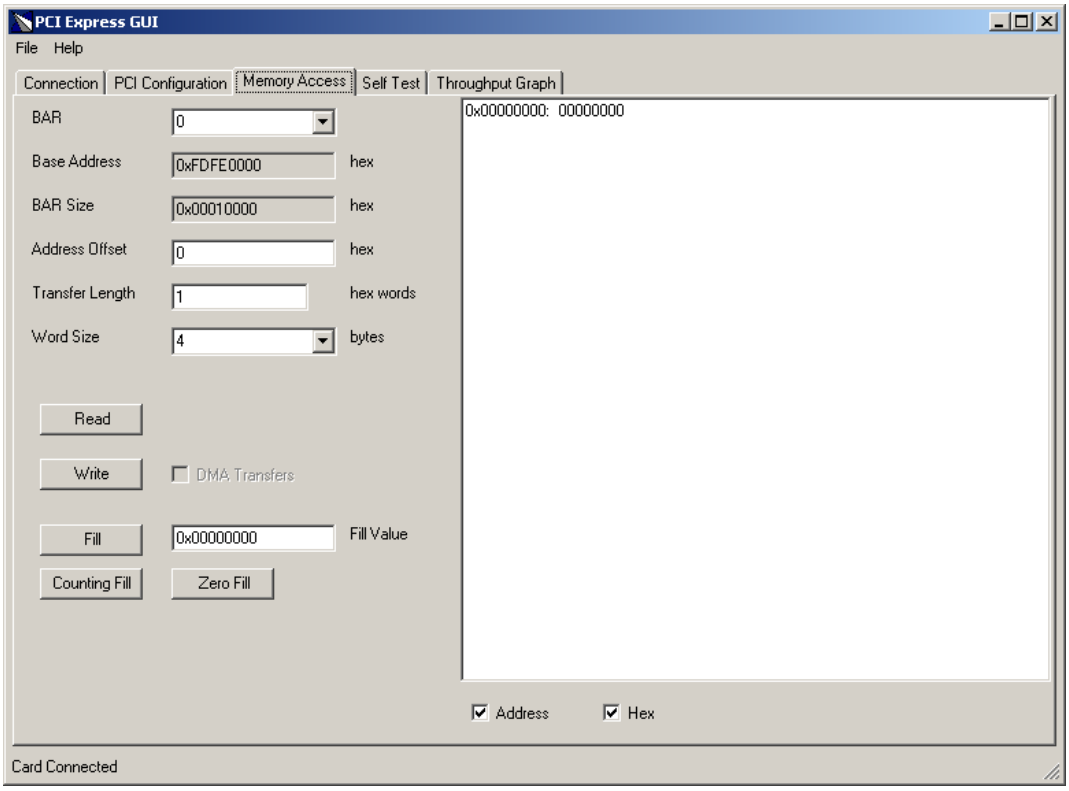

Figure 11: PciExpress – Memory Access Page

To directly read and write memory, switch to the **Memory Access** tab. Select BAR1. To read a block, enter the start address ("offset"), length, and word size, and press **Read**. To write memory, set the parameters as before, then press either **Counting Fill, Zero Fill,** or **Fill** (after setting a **Fill Value**). Then press **Write** to actually write the displayed data into memory.

Register access is through BAR0. Reading 8000-803F will show some internal identification constants. Try writing location 8040. You will see the lower nibble reflected in the ViClaro's LEDs!